AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of driving a liquid crystal display device, the liquid crystal display device comprising driver circuit, which comprises a timing controller driven by a data ~~transmission~~ reception signal (~~LOAD~~ DSTH signal) and a source driver driven by a data ~~reception~~ transmission signal (~~DSTH~~ LOAD signal), the method comprising the steps of:

detecting a status of the LOAD signal; and

controlling a DCLK signal according to the status of the LOAD signal.

2. (Currently amended) A method of driving a liquid crystal display device, the liquid crystal display device comprising a driver circuit, which comprises a timing controller driven by a data ~~transmission~~ reception signal (~~LOAD~~ DSTH signal) and a source driver driven by a data ~~reception~~ transmission signal (~~DSTH~~ LOAD signal), the method being characterized in that:

within the period from the time when the data transmission signal (LOAD signal) is enabled to the time when the data reception signal (DSTH signal) is enabled, a data clock (DCLK signal) is forced to be at a low voltage level.

3. (Original) The method of claim 2, wherein the LOAD signal is enabled at a high voltage level.

4. (Original) The method of claim 3, wherein forcing the DCLK signal to be at a low voltage level begins at the rising edge of the LOAD signal when being as a high voltage level.

5. (Original) The method of claim 3, wherein forcing the DCLK signal to be at a low voltage level begins at the falling edge of the LOAD signal when being as a high voltage level.

6. (Original) The method of claim 2, wherein the DSTH signal is enabled at a high voltage level.

7. (Original) The method of claim 6, wherein forcing the DCLK signal to be at a low voltage level ends at the falling edge of the DSTH signal when being as a high voltage level.

8. (Original) The method of claim 6, wherein forcing the DCLK signal to be at a low voltage level ends at the rising edge of the DSTH signal when being as a high voltage level.

9. (Currently amended) A method of driving a liquid crystal display device, the liquid crystal display device comprising driver circuit, which comprises a timing controller driven by a data ~~transmission~~ reception signal (~~LOAD~~ DSTH signal) and a source driver ~~drived~~ driven by a data ~~reception~~ transmission signal (~~DSTH~~ LOAD signal), the method comprising the steps of:

detecting the status of the LOAD signal to determine whether the data input begins;

forcing a DCLK signal to be at a low voltage level when the LOAD signal is at a high voltage level;

detecting the status of the DSTH signal to determine whether the data input is completed; and

returning the DCLK signal to be at a normal voltage level when the DSTH signal is detected.

10. (Original) The method of claim 9, wherein the LOAD signal is enabled at a high voltage level.

11. (Original) The method of claim 10, wherein forcing the DCLK signal to be at a low voltage level begins at the rising edge of the LOAD signal when being as a high voltage level.

12. (Original) The method of claim 10, wherein forcing the DCLK signal to be at a low voltage level begins at the falling edge of the LOAD signal when being as a high voltage level.

13. (Original) The method of claim 9, wherein the DSTH signal is enabled at a high voltage level.

14. (Original) The method of claim 13, wherein forcing the DCLK signal to be at a low voltage level ends at the falling edge of the DSTH signal when being as a high voltage level.

15. (Original) The method of claim 13, wherein forcing the DCLK signal to be at a low voltage level ends at the rising edge of the DSTH signal when being as a high voltage level.

16. (New) A method of driving a liquid crystal display device, the liquid crystal display device comprising a driver circuit, which comprises a timing controller and a source driver wherein the timing controller is driven by a data reception signal (DSTH signal) to receive image data, and outputs a data transmission signal (LOAD signal) and a digital image signal according to the image data, and the source driver is driven by the data transmission signal (LOAD signal) to receive the digital image signal, the method comprising the steps of:

detecting the status of the LOAD signal to force a DCLK signal to be at a low voltage level when the LOAD signal is at a high voltage level; and

detecting the status of the DSTH signal to return the DCLK signal to be at a normal voltage level when the DSTH signal is detected.

17. (New) The method of claim 16, wherein the LOAD signal is enabled at a high voltage level, and forcing the DCLK signal to be at a low voltage level begins at the rising edge of the LOAD signal when being as a high voltage level.

18. (New) The method of claim 16, wherein the LOAD signal is enabled at a high voltage level, forcing the DCLK signal to be at a low voltage level begins at the failing edge of the LOAD signal when being as a high voltage level.

19. (New) The method of claim 16, wherein the DSTH signal is enabled at a high voltage level, forcing the DCLK signal to be at a low voltage level ends at the falling edge of the DSTH signal when being as a high voltage level.

20. (New) The method of claim 16, wherein the DSTH signal is enabled at a high voltage level, forcing the DCLK signal to be at a low voltage level ends at the rising edge of the DSTH signal when being as a high voltage level.